WIZTECH AUTOMATION SOLUTIONS (P) LTD.,

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VLSI Course Details

INTRODUCTION TO VLSI

- VLSI Design Flow
- ASIC vs FPGA
- RTL Design Methodologies

ADVANCED DIGITAL DESIGN

- Introduction to Digital Electronics
- Arithmetic Circuits
- Data Processing Circuits
- Combinational Circuits– Design and Analysis
- Sequential Circuits– Design and Analysis
- Memories and PLD
- Finite State Machine

VHDL

- VHDL Overview and Concepts
- Levels of Abstraction
- Entity, Architecture
- Data Types and declaration
- Enumerated Data Types
- Relational, Logical, Arithmetic Operators
- Signal and Variables, Constants
- Process Statement
- Concurrent Statements
- When-else, With-select

- Sequential Statement
- If-then-else, Case
- Slicing and Concatenation
- Loop Statements
- Delta Delay Concept
- Arrays, Memory Modeling, FSM
- Writing Procedures
- Writing Functions
- Behavioral / RTL Coding
- Operator Overloading
- Structural Coding
- Component declarations and installations
- Generate Statement
- Configuration Block
- Libraries, Standard packages
- Local and Global Declarations
- Package, Package body
- Writing Test Benches

VERILOG

- Language introduction
- Levels of abstraction
- Module, Ports types and declarations
- Registers and nets, Arrays
- Identifiers, Parameters
- Relational, Arithmetic, Logical, Bit-wise shift Operators
- Writing expressions
- Behavioral Modeling
- Structural Coding

- Continuous Assignments
- Procedural Statements
- Always, Initial Blocks, begin end, fork join
- Blocking and Non-blocking statements
- Operation Control Statements
- If, case
- Loops: while, for-loop, for-each, repeat
- Combination and sequential circuit designs
- Memory modeling,, state machines
- CMOS gate modeling
- Writing Tasks
- Writing Functions

- Compiler directives
- Conditional Compilation
- System Tasks
- Gate level primitives
- User defined primitives
- Delays, Specify block
- Testbenches, modeling, timing checks

SYSTEM VERILOG

- Introduction to SystemVerilog
- Applications of SystemVerilog
- Literal values
- Arrays, Data Types
- Data Declarations
- Attributes, Operators and Expressions
- Procedural Statements & Control Flow
- Processes, Tasks and Functions
- Classes, Random Constraints
- Inter Process Synchronization Communication
- Scheduling Semantics
- Clocking block, Program block
- Assertions, Hierarchy
- Interfaces, Coverage
- Parameters, Configuration Libraries
- System Tasks and Functions, Compiler directives
- Direct Programming Interface (DPI)
- SystemVerilog Assertion

VMM METHODOLOGY

- VVM tutorial
- Examples

UVM METHODOLOGY

- UVM tutorial
- Examples

OVM METHODOLOGY

- OVM tutorial
- Examples